Evaluating Defects in Solution-Processed Carbon Nanotube Devices *via* Low-Temperature Transport Spectroscopy

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ARTICLE

ABSTRACT We performed low-temperature electron transport spectroscopy to evaluate defects in individual single-walled carbon nanotube (SWNT) devices assembled *via* dielectrophoresis from a surfactant-free solution. At 4.2 K, the majority of the devices show periodic and well-defined Coulomb diamonds near zero gate voltage corresponding to transport through a single quantum dot, while at higher gate voltages, beating behavior is observed due to small potential fluctuations induced by the substrate. The Coulomb diamonds were further modeled using a single electron transistor simulator. Our study suggests that SWNTs derived from stable solutions in this work are free from hard defects and are relatively clean. Our observations have strong implications on the use of solution-processed SWNTs for future nanoelectronic device applications.

KEYWORDS: solution-processed · single electron transistor · nanotube · electron transport · transport spectroscopy · defects

The unique electronic properties of single-walled carbon nanotubes (SWNTs) make them promising candidates for future nanoelectronic devices.[1,2] Fabrication of high-quality and high-performance SWNT devices requires clean SWNTs with a minimal amount of defects. To date, the most widely used technique to achieve clean and high-quality SWNT devices involves chemical vapor deposition (CVD) growth of SWNTs directly on the substrate and then making electrical contact to them without further processing (direct growth method). This is done by randomly dispersed catalytic particles or lithographically patterned catalytic islands for which the latter allows for parallel fabrication of SWNT devices at selected position of the circuit with high yield.[3,4] Electronic transport measurements on such devices revealed transistors with mobilities typically ranging from 1000 to 10 000 $cm^2/(V \cdot s)$[5] and conductance nearing the ballistic limit ($G = 4e^2/h \sim$ 155 μS or $R \sim 6.5$ kΩ).[6] Further low-temperature electronic transport studies on individual SWNTs have shown evidence of clean quantum dots (QDs),[7] long mean free paths (up to 4 μm),[8] and the observation of novel quantum phenomenon such as Kondo effects,[9] Wigner crystallization,[10] Franck−Condon blockade,[11] Mott insulators,[12] spin−orbit coupling,[13] and ultraclean double QDs,[14] providing a strong indication of clean and defect-free SWNT devices. Although high-quality devices have been obtained using direct growth CVD technique, CVD requires high growth temperatures (900 °C), which is not compatible with current complementary metal−oxide−semiconductor (CMOS) fabrication technologies.

An attractive alternative to the direct growth technique for the high-throughput assembly of electronic devices at selected positions of the circuit is from post-synthesis fabrication using solution-processed SWNTs.[15−31] Solution processing could be advantageous due to its ease of processing at room temperature, CMOS compatibility, and potential for scaled up manufacturing of SWNT devices on various substrates. To fabricate individual SWNT devices from solution with high yield, it is necessary that (1) individual SWNTs are dispersed (debundled) and stabilized in the solution and (2) impurities such as catalytic particles and amorphous carbon from the growth procedure are removed.[17,18] Common techniques that are implemented in achieving these goals are noncovalent adsorption or covalent functionalization. The former typically involves encapsulating the SWNTs with surfactants using long, aggressive sonication times, while the latter entail functionalization to the SWNT side wall through acid treatments that introduce carboxylic groups which separate bundles

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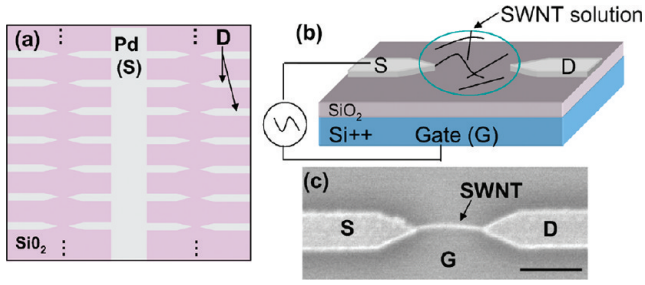

Figure 1. (a) Top view schematic for a portion of the electrode array showing the common Pd source electrode (S) and independent drain electrodes (D). (b) Three-dimensional illustration of DEP assembly on adjacent taper-shaped electrodes. (c) Resulting scanning electron micrograph (SEM) of an individual SWNT assembled between the electrode pair. Scale bar: 1 μm.

and stabilize suspensions. Over the past few years, there has been tremendous effort and continuous progress in producing high-quality SWNT stable solutions.[19−21] This has led to the sorting of metallic and semiconducting SWNTs[22] and the commercialization[23,24] of electronic grade SWNT solutions. It is, however, generally believed that solution processing techniques can introduce defects and degrade the intrinsic electrical properties of SWNTs, which in turn could limit their application in high-quality nanoelectronic devices.

Up until now, solution-processed SWNTs have been mostly characterized by Raman spectroscopy and room temperature electrical transport measurements. Although Raman spectroscopy has been done on a number of individual SWNTs derived from stable suspensions and shows an absence or a reduction of a D-band resonance (defect related band) implying relatively defect-free SWNTs,[25,26] it was noted that Raman spectroscopy is not sensitive enough to low defect densities and therefore may not provide an accurate picture.[27,28] Room temperature electron transport studies of individual solution-processed SWNT devices show moderate device properties compared to devices from direct growth techniques, such as maximum on-state conductance of ($G_{on} \sim 1$ μS)[29] and mobility up to 67 $cm^2/(V \cdot s)$.[30] However, it is not clear whether the moderate device properties stem from poor contact or are due to defects in SWNTs. Only in strongly disordered SWNTs, room temperature electron transport measurements will reveal obvious effects. For SWNTs with low defect densities, only at low temperature will disorder become dominant as a scattering mechanism. Low-temperature electron transport spectroscopy serves as a powerful technique to evaluate defects in nanostructures.[32,33] However, there are almost no systematic low-temperature transport spectroscopy studies done on SWNT devices assembled from stable solutions of SWNTs. If there are several defects along a SWNT, they will act as tunnel barriers and lead to many QDs in series which will show irregular Coulomb diamonds with multiple energy scales. On the other hand, if there are no defects, the entire SWNT between two electrodes can act as a single QD provided the contacts act as tunnel barriers and lead to periodic Coulomb oscillations with well-defined Coulomb diamonds as a function of gate voltage.

In this paper, we utilize low-temperature transport spectroscopy on individual solution-processed SWNTs assembled by dielectrophoresis between 1 μm spaced Pd source and drain electrodes to systematically evaluate the defects in many SWNT devices. We show that, at 4.2 K, the majority of the devices display periodic and well-defined Coulomb diamonds at low gate voltage regimes, indicating single QD behavior, while at higher gate voltage regimes, beating behavior is observed due to small potential fluctuations in the SWNT. The Coulomb diamonds were modeled in each gate voltage regime using a commercially available SET Monte Carlo simulator to determine the number of QDs in the channel. Our observations suggest that the SWNTs derived from stable solutions in this study are free from hard defects and are relatively clean. These results are an important step forward for the use of solution-processed SWNTs for high-yield and high-quality devices in nanoelectronics.

RESULTS AND DISCUSSION

The devices were fabricated on highly doped Si substrates with a 250 nm thick SiO_2 caped layer (see Materials and Methods for more details). Figure 1a shows a top view schematic of a portion of the electrode array for the DEP assembly. The gray Pd electrode in the middle is the common source electrode (S), and the adjacent electrodes are independent drain electrodes (D). A stable, surfactant-free solution of SWNTs was obtained from Brewer Science for the assembly.[23] Figure 1b shows a 3D cartoon of the assembly setup where we apply the AC voltage between the common source electrode and the back gate. In this way, each drain electrode became capacitively coupled to the gate electrode and obtained a similar potential as the gate, creating the necessary potential difference between each source and drain electrode to align the SWNTs simultaneously between each pair.[29]

Figure 1c shows a scanning electron micrograph (SEM) of an individual SWNT assembled between a source and drain electrode pair. The total yield of individual SWNTs at low concentration was ~20% on average and as high as 35% for a single chip, which is consistent with similar DEP studies.[34,35] The average diameter of the assembled SWNTs presented in this paper was ~2.0 ± 0.3 nm, as determined by atomic force microscopy (AFM) (see Supporting Information Figure S1). The average two-terminal resistance of the devices after annealing was ~1 MΩ, and for certain devices, it was as low as ~60 kΩ.

The devices were then bonded and loaded into a ^{4}He cryostat for electronic transport measurements.

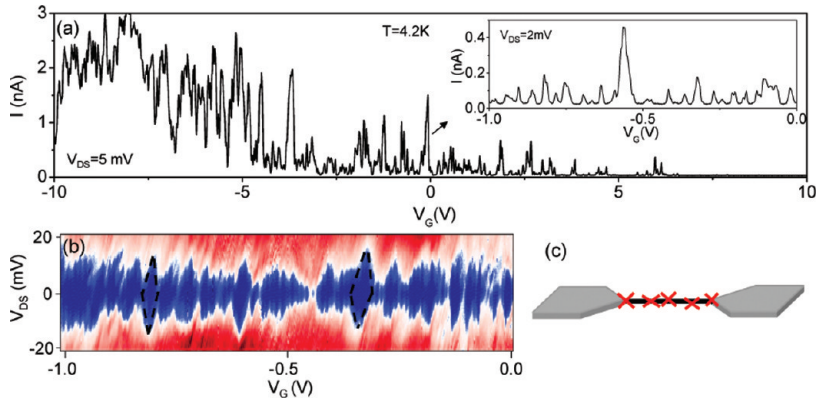

Figure 2. Device A: (a) *I versus* V_G with $V_{DS} = 5$ mV for entire gate voltage range at $T = 4.2$ K showing Coulomb oscillations. Inset: Expanded view of irregular Coulomb oscillations with $V_{DS} = 2$ mV. (b) Color scale plot of differential conductance (dI/dV_{DS}) as a function of V_G and V_{DS} for a selected gate voltage range at 4.2 K, showing irregular diamond patterns outlined by black dashed lines. (c) Possible scenario of defects (red crosses) that lie along the tube.

We performed measurements on a total of 16 individual SWNT devices. As verified though room temperature transport measurements, 11 of the devices were metallic or small band gap SWNTs (*i.e.*, showed less than 1 order of magnitude change in current (I) as a function of gate voltage (V_G)) and 5 of the devices show semiconducting behavior (1 or more orders of magnitude change in I as a function of V_G). Here we show transport measurements on six representative devices (A−F). The room temperature transport data for these devices are presented in Supporting Information Figure S2.

Figure 2a shows I plotted *versus* V_G at $T = 4.2$ K with $V_{DS} = 5$ mV for device A, a representative sample with strong disorder. Current oscillations are observed as a function of gate voltage, typical of single electron transistor behavior.[33] The inset in Figure 2a shows an expanded view of current oscillations from -1.0 V $< V_G < -0.0$ V with $V_{DS} = 2$ mV. Here it can be seen that the oscillations are *not* periodic in V_G. Figure 2b is a color scale plot of differential conductance (dI/dV_{DS}), plotted as a function of both V_{DS} and V_G taken at 4.2 K (often called a *stability plot*). The conductance was calculated by numerically differentiating the $I-V_{DS}$ curves for different gate voltages. Brighter regions (red and white) symbolize high conductance, and darker regions (blue) signify Coulomb blockade. Several irregular diamond-shaped regimes (Coulomb diamonds, outlined by black dashed lines) of different height can be seen. The diamonds do not close, and the slopes are not constant. The irregular Coulomb oscillations and irregular diamonds with no closing are typical of charge transport through multiple QDs[33] defined by a number of defects along the nanotube.[36] The height of the Coulomb dia-

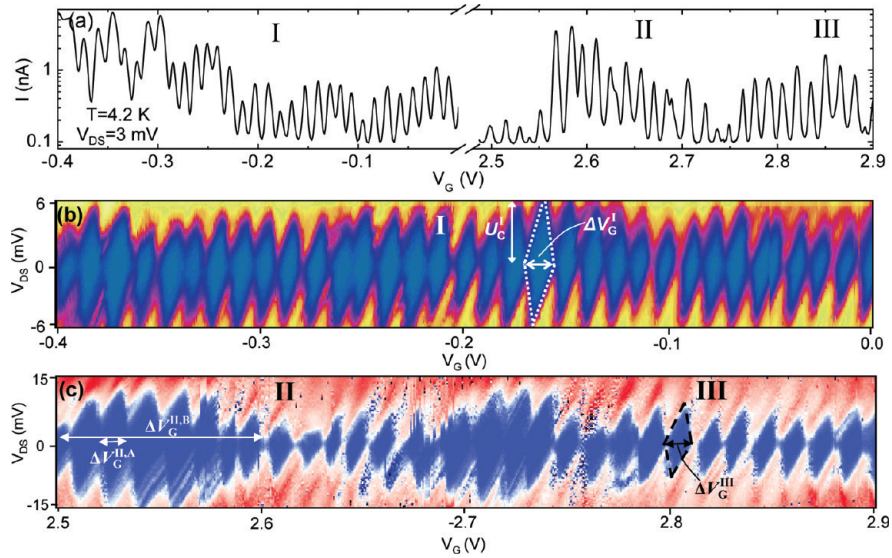

Figure 3. Device B: (a) Current *versus* gate voltage at $V_{DS} = 3$ mV and $T = 4.2$ K in three different gate voltage regions (regions I, II, and III). (b) dI/dV_{DS} as a function of V_G and V_{DS} at 4.2 K in region I. Coulomb diamonds (outlined by white dotted lines on the right) showing equal spacing (ΔV_G). The charging energy, U_C, is the height of the diamond. Bright regions symbolize high conductance, and dark regions symbolize low conductance or Coulomb blockade. (c) Stability plot in regions II and III. A "beating" behavior is observed in region II, whereas in region III, there are clear closing diamonds with constant charging energy.

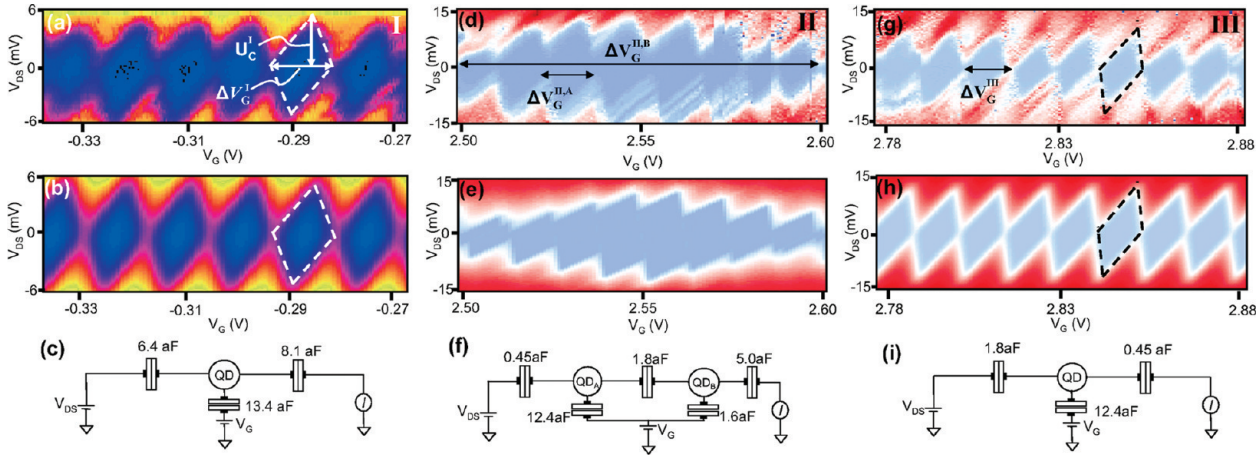

Figure 4. (a) Expanded view of the stability plot in region I for device B. (b) Simulated stability plot of the same gate voltage range. (c) Single quantum dot circuit diagram used for the simulation in panel b. (d) Expanded view of the stability plot in region I showing beating behavior. (e) Simulated stability plot using two QDs in series. (f) Circuit diagram of two QDs in series. (g) Expanded stability plot in region III, where single QD behavior is observed once again. (h) Simulated stability plot for a single QD using the parameters extracted from panel g. (i) Single QD circuit diagram used for the simulation in panel h.

mond is a measure of the charging energy (U_c) for the quantum dot, which varies from ~10 to 20 meV for this device. From the charging energy, we estimated the size (L) of the QDs along the SWNT using $U_c \sim 5.0$ meV/$L(\mu m)$[37] and obtained the sizes of the QDs varying between ~0.25 and 0.50 μm. In Figure 2c, we depict a possible model of this device where we show multiple defect locations along the SWNT. This in turn leads to a number of QDs in series and creates the disordered-like transport signatures. For this sample, we did not observe any periodic oscillations or clean diamond for any gate voltage regime.

We now present measurements on device B, a representative of a relatively clean SWNT device. Figure 3a shows $I-V_G$ characteristics for three representative gate voltage regions; -0.4 V $< V_G < 0$ V (region I), 2.50 V $< V_G <$ 2.75 V (region II), and 2.75 V $< V_G <$ 2.90 V (region III). It can be seen here that, unlike device A, this device showed periodic Coulomb oscillations in these gate voltage ranges. At gate voltages less than $V_G = -0.4$ V, the same period of oscillations still persists but is accompanied by broader oscillations. From 0 V $< V_G <$ 2.5 V, oscillations similar to region I are observed, and at some gate voltages above $V_G = 2.9$ V, a similar period of oscillations to region I exists but then becomes irregular at $V_G > 6$ V.

Figure 3b shows the stability plot for region I. Many regular and well-defined Coulomb diamonds (shown by the dashed lines) are seen with regular spacing ($\Delta V_G^I \sim 12$ mV). Figure 3c shows the stability plot from regions II and III. In region II, an interesting beating behavior is observed. Here the diamonds are not quite closing, and there are several smaller diamonds with $\Delta V_G^{II,A} \sim 13$ mV (similar to region I) beating in a larger diamond with $\Delta V_G^{II,B} \sim 100$ mV. However, in region III, Coulomb diamonds with constant charging energy and periodic spacing ($\Delta V_G^{III} \sim 13$ mV), similar to that of region I, reappeared. To further understand the details of this transport behavior, we fitted the data using a commercially available Monte Carlo single electron transistor simulator (SIMON 2.0).[38]

Figure 4a shows an expanded portion of the stability plot from region I. In Figure 4b, we show the simulated data using a single QD model (depicted in Figure 4c) with gate capacitance of $C_G^I = e/\Delta V_G^I \sim 13.4$ aF. The source and drain capacitance are found from the slopes of the diamonds which yield values of $C_S^I \sim 6.4$ aF and $C_D^I \sim 8.1$ aF, respectively.[39] The modeled data fit well with the experiment, indicating measurement of a single QD for this region. We find that the total capacitance in region I is $C_\Sigma^I = C_S^I + C_D^I + C_G^I = 27.9$ aF and calculate a charging energy of $U_C^I = e^2/C_\Sigma^I \sim 5.8$ meV, which is consistent with the value directly read off of the stability diagram from the diamond height in Figure 4a. We estimated the size of the QD to be $L_I = 5$ meV/$U_C^I \sim 0.860$ μm, in close agreement with the spacing between the source and drain electrodes, which was defined to be 1.0 μm during fabrication. This strongly suggests that the observed behavior in region I stems from a single QD defined by the source and drain electrodes and not a pair of defects along the tube (discussed in more detail below).

Figure 4d shows an expanded view of the stability plot in region II. We found that the beating behavior could not be explained by a single QD model and that the data fit best with two QDs in series, as shown by the simulation in Figure 4e. Figure 4f shows a circuit diagram of the two QDs in series where we used $C_G^{II,A} = e/\Delta V_G^{II,A} = 12.4$ aF (smaller diamonds, QD_A) and $C_G^{II,B} = e/\Delta V_G^{II,B} = 1.6$ aF (larger diamond, QD_B). The source and drain capacitances are $C_S^{II} = 5.0$ aF and $C_D^{II} = 0.45$ aF, respectively, and the capacitance between the two QDs is $C_{A,B} = 1.8$ aF. The beating pattern disappears when continuing to region III (Figure 4g), where we again observe single QD behavior with clean and well-defined closing diamonds. In region III, the data fit well again

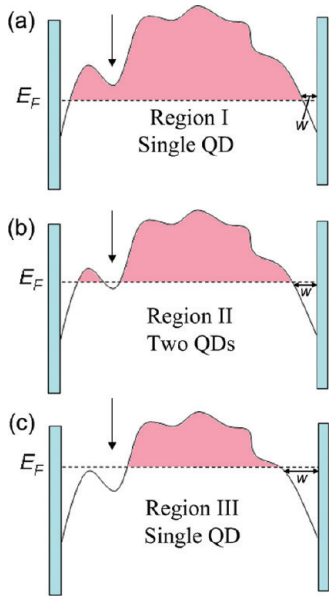

Figure 5. Possible band diagram model for device B in regions I, II, and III.

with a single QD model using $C_G^{III} = 12.4$ aF, $C_S^{III} = 1.8$ aF, and $C_D^{III} = 0.46$ aF, as shown Figure 4h,i. These values are identical to the capacitance values from QD_A in region II, suggesting that QD_A is dominating the transport in regions II and III but is accompanied by a small perturbation in region II.

Beating effects have been observed previously in Si quantum wires as well as SWNT QDs.[40−44] For Si quantum wires, the behavior is thought to stem from QDs in series due to inhomogeneous doping. Similar behavior in potassium-doped SWNT QDs has also been explained in the same way.[42] This is highly unlikely in our case because no dopants were used in this experiment. Park *et al.* and Babic *et al.* explained the beating pattern in an ambipolar SWNT QD by a small p-type QD forming at the end of an n-type SWNT near the contact and therefore forming two serial QDs at positive gate voltages.[43,44] However, in our experiment, only p-type behavior at 4.2 K was observed.

Therefore, we suggest that the evolution from single QD behavior to two serial QDs and back to single QD behavior in sample B is due to local potential fluctuations along the SWNT that perturb the overall band structure, as depicted in Figure 5, where we show a possible band configuration for regions I, II, and III. In region I (Figure 5a), the potential fluctuations are all above the Fermi level (E_F), hence forming a single QD. As the gate voltage is increased, raising E_F, we enter into region II (Figure 5b), where one of the fluctuations (indicated by arrow) near the contact forms two QDs in series. By increasing the gate voltage slightly further, E_F lies above the potential fluctuation (Figure 5c) and hence gives rise to single QD behavior again. This model is also consistent with the observation that the gate capacitance remains the same in all regions, while the source and drain capacitances decreased as we moved to II and III (see above). C_S and C_D decrease by almost an order of magnitude for region III compared to region I, which is evidence for the thickening of the Schottky barriers (w) as V_G increases, as shown in Figure 5.[45−47]

We observed behavior similar to that of device B in several other devices. Figure 6 shows the $I-V_G$ curves and stability diagrams of four other devices (C, D, E, F) measured at 4.2 K, which show single QD behavior near $V_G \sim 0$ V. At higher gate voltages, these devices showed transport properties similar to those of device B (not shown here). The stability plots for all of these samples yield comparable charging energy as device B (~6.0 meV) and similar QD size (~0.80 μm) near $V_G \sim 0$ V, which is also summarized in Table 1, where we list the

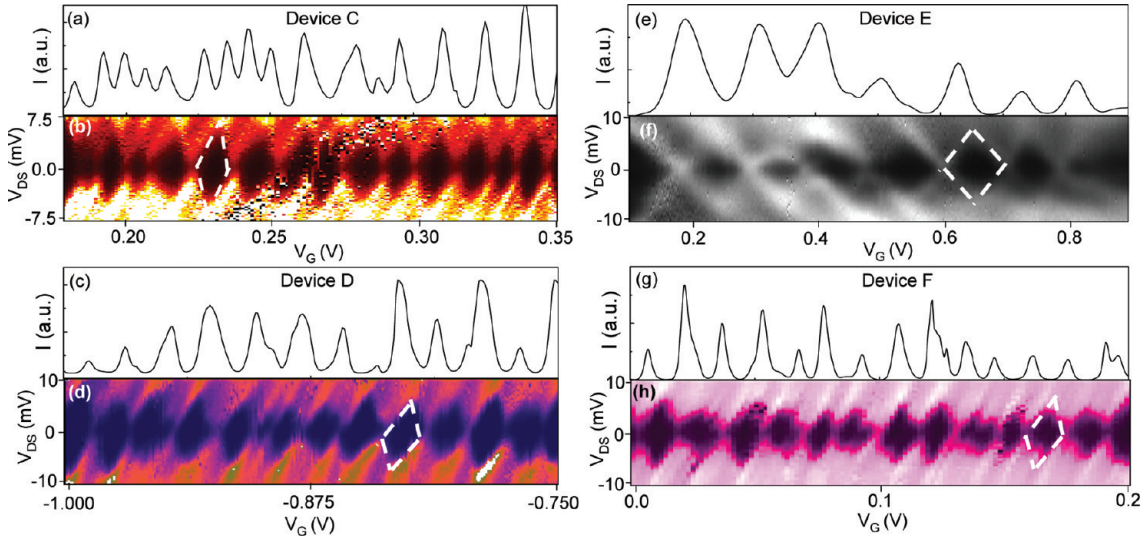

Figure 6. Device C, D, E, and F. Plots of current as a function of gate voltage and stability plot for several other semimetallic SWNT devices. All of the devices show relatively periodic Coulomb oscillations and transport spectra near $V_G \sim 0$ V with similar charging energy, demonstrating the reproducibility from device to device.

TABLE 1. Summary of Coulomb Diamond Spacing ΔV_G, Gate Capacitance (C_G), Source (C_S) and Drain (C_D) Capacitance, Charging Energy (U_C), and Calculated Sizes (L) from $L = 5$ meV/U_C

device	ΔV_G (mV)	C_G (aF)	C_S (aF)	C_D (aF)	U_C (meV)	L (μm)
B	12.0	13.4	6.4	8.1	5.8	0.86
C	10.1	16.2	9.3	0.3	6.3	0.80
D	13.8	11.7	5.2	10.2	6.0	0.84
E	76.1	2.1	15	8.6	6.3	0.80
F	11.3	14.3	11	0.2	6.3	0.80

capacitances, charging energy, and QD size for devices B−F.

We now discuss the possible origin of the potential fluctuations shown in Figure 5. Disorder in SWNTs can arise through a number of different ways, such as (1) mechanical deformations, (2) intrinsic defects from growth or processing (hard defects), and (3) electrostatic potential fluctuations by random charges in the substrate (soft defects).[48] Bends and buckles can lead to tunnel barriers in SWNT devices and introduce QDs.[49−52] However, our devices do not show any evidence of mechanical bending from the SEM images. Defects such as localized lattice vacancies due to volatile processing or substitutions in the lattice from growth are also a possibility. However, defects such as these lead to short-range scattering from sharp delta-like potentials and significantly modify the electron transport properties, and therefore, it would be difficult to observe single QD behavior for any gate voltage range.[53] We also rule this possibility out because we observed similar transport behavior to device B in a number of other devices as discussed above. It is highly improbable that, in each device, a pair of hard defects from growth or processing would occur the same distance away along the SWNT and give rise to the same charging energy.

As a result, we propose that the potential fluctuations stem from random localized charges in the substrate. This is supported by several experimental evidence and has been accredited for disorder in SWNTs from direct growth methods also.[7] First, on the second cool down of device B (see Supporting Information Figure S3a,b) and a few other samples, the same charging energy and gate capacitances as that of first cool down were observed, which further confirms that the effective QDs formed in all of these devices are defined by the permanent tunnel barriers at the source and drain electrodes. Second, although a beating pattern for device B was observed in the second cool down, it did not appear in the same voltage range as that of the first cool down (see Supporting Information Figure S4a). This suggests that the beating behavior was most likely due to a temporary impurity in the substrate or charge trap that was frozen into the system.

Out of the 16 total devices we measured, approximately 70% of small band gap or metallic devices and 20% of the semiconducting (large band gap) devices showed transport characteristics similar to device B. The remaining small band gap or metallic devices and large band gap semiconducting devices showed multiple quantum dot behavior similar to device A. This is most likely due to a larger amount of long-range scattering sites stemming from a higher density of charge traps in the substrate and is consistent with previous studies of suspended SWNT devices by direct growth methods, where it was found that 20−30% of the small band gap SWNT devices showed disordered transport behavior.[7] The disordered transport in the semiconducting devices with large band gaps is consistent with theoretical and experimental studies that showed transport properties of semiconducting SWNTs have a stronger sensitivity to disorder.[36,54] The effect of charge traps from the substrate can be further confirmed by low-temperature transport spectroscopy of suspended solution-processed SWNTs, and work is in progress to that end.

In conclusion, we evaluated defects in individual solution-processed SWNT devices assembled by DEP *via* low-temperature electron transport spectroscopy. The majority of the devices show periodic and well-defined Coulomb diamonds at low gate voltage regime corresponding to transport through a single QD, while at higher gate voltage regimes, beating behavior is observed due to potential oscillations induced by the substrate. The Coulomb diamonds in different regimes were further modeled using a commercially available SET Monte Carlo simulator. We present a possible band diagram model to explain the beating behavior. Our observations suggest that a majority of the SWNT devices derived from stable solutions in this study are free from hard defects and are relatively clean. This is a significant step forward for the use of solution-processed SWNTs for high-yield and high-quality devices in nanoelectronics.

MATERIALS AND METHODS

Larger electrode patterns and contact pads were fabricated by standard optical lithography followed by thermal deposition of 3 nm Cr and 50 nm thick Au. Smaller source and drain electrode pairs with a 1 μm gap were defined using electron beam lithography (EBL) and subsequent electron beam deposition of 2 nm Cr and 25 nm thick Pd followed by lift-off. There are 28 independent drain electrodes on each chip.

Prior to assembly, the sample was placed in oxygen plasma cleaner for 10 min to remove the unwanted organic residues on the surface. The Brewer Science solution had a shelf life of 6 months and a concentration of SWNTs ~ 50 μg/mL. The solution consists of mostly individual SWNTs and was free of catalytic particles. The average length of the SWNTs was ~1−2 μm as determined by scanning electron microscopy (SEM). After dilution of the solution to ~10 ng/mL, a 3 μL drop was cast onto the electrode array. An AC voltage of 5 Vp-p at 1 MHz was applied between the source and gate electrode for 3 min, keeping the drain electrodes floating. Subsequently, the drop of solution was blown off the chip with nitrogen gas.

The annealing of the devices was done in a 3 in. tube furnace. A flow of ~200 cc/min of ultrahigh pure argon and ~2000 cc/min ultrahigh pure hydrogen was initiated and left running for a few minutes to purge the system. The furnace was then heated to 200 C for 1 h and then turned off. During cool down of the furnace, both argon and hydrogen flows were maintained until the furnace reached room temperature, and then the gases were turned off and the samples were removed.

The devices were imaged using a Zeiss Ultra 55 SEM and a Veeco Dimension 3100 AFM in tapping-mode. DC charge transport measurements were performed by means of a DL instruments 1211 current preamplifier and a Keithley 2400 sourcemeter interfaced with LabView.

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Supporting Information Available: AFM height measurement, room temperature current−gate voltage characteristics, and stability plots for device B on the second cool down. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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